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Substitute for Form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			Complete If Known		
			Application Number	09/976,983	
			Filing Date	10/12/2001	
			First Named Inventor	Xiaowei Deng, et al.	
			Group Art Unit	2518	
			Examiner Name	PHAN	
Sheet	1	of	1	Attorney Docket No	TI-31071

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09/976983  
PTO

U.S. PATENT DOCUMENTS

Exam. Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
TP	AA	6,044,011		MARR, et al.	03/28/2000	365/154
	AB					
	AC					
	AD					
	AE					
	AF					
	AG					
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	AI					
	AJ					

FOREIGN PATENT DOCUMENTS

Exam. Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>2</sup> (if known)				
	BA							
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Exam Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
TP	CA	NODA, K., et al., "A 1.9- $\mu\text{m}^2$ Loadless CMOS Four-Transistor SRAM Cell in a 0.18- $\mu\text{m}$ Logic Technology," 1998 IEEE, pp. 643-646	
TP	CB	NODA, K., "An Ultra-High-Density High-Speed Loadless Four-Transistor SRAM Macro with a Dual-Layered Twisted Bit-Line and a Triple-Well Shield," 2000 IEEE Custom Integrated Circuits Conference, pp. 283-286	
TP	CC	TAKEDA, KOICHI, et al., "A 16Mb 400MHz Loadless CMOS Four-Transistor SRAM Macro," 2000 IEEE International Solid-State Circuits Conference, 2/8/2000, Digest of Technical Papers, pp. 264-265	
TP	CD	MASUOKA, S., et al., "A 0.99- $\mu\text{m}^2$ Loadless Four-Transistor SRAM Cell in 0.13- $\mu\text{m}$ Generation CMOS Technology," IEEE 2000 Symposium on VLSI Technology, Digest of Technical Papers, pp. 164-165	
	CE		
	CF		
	CG		
	CH		
	CI		
	CJ		

Examiner Signature	Trang Phan	Date Considered	3/4/02
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